REMARKS

Claims 1-8, 10, 12 and 13 are now present in this application.

Claims 1, 5 and 10 have been amended, and claims 9 and 11 have been cancelled without prejudice or disclaimer of the subject matter contained therein. Reconsideration of the application, as amended, is respectfully requested.

Claim 5 stands rejected under 35 USC 112, second paragraph. This rejection is respectfully traversed.

In view of the foregoing amendments, it is respectfully submitted that the claims particularly point out and distinctly claim the subject matter of the instant invention. More specifically, in amended claim 5, "wherein the delay from the first input signal to the reset of the phase error detecting unit is substantially the same as the delay from the first input signal to the first flag signal" has been changed to --wherein the time from a state transition of the first input signal to a corresponding reset of the phase error detecting unit is substantially the same as the time from the state transition of the first input signal to a corresponding state change of the first flag signal.-- As would be understood by a person of ordinary skill in the art, and is fully supported by the originally filed specification, a temporal difference (i.e., delay) between a state transition (for example, a rising edge) of the first input signal and a corresponding occurrence of reset of the phase error detecting unit is substantially the same as a temporal difference between the state change of the first input signal and a corresponding state transition of the first flag signal, as set forth in amended claim 5.

Claims 1-4, 6, 7 and 9-11 stand rejected under 35 USC 102(b) as being anticipated by Tsinker, U.S. Patent 6,323,692. This rejection is respectfully traversed.

Claims 1, 2, 8 and 9 stand rejected under 35 USC 102(b) as being anticipated by Lee et al., U.S. Patent 6,326,826. This rejection is respectfully traversed.

With regard to the patent to Tsinker, it is noted that the limitations of claims 9 and 11 have been incorporated into independent claims 1 and 10, respectively.

Independent claims 1 and 10 now recite the limitation of:

"wherein the reset unit resets the phase error detecting unit such that the length of the phase error signal has a substantial linear relationship with the phase error of the first input signal and the second input signal;"

Although the Examiner has rejected dependent claims 9 and 11, which originally set forth this limitation, it is respectfully submitted that Tsinker fails to teach the above noted limitation. First, in page 4, lines 1 and 12, of the Office Action, the Examiner sets forth that Tsinker also meets the above noted limitation, but does not referr to any specific disclosure in Tsinker, nor providing any specific rationale. It is respectfully submitted that the Examiner has failed to establish a prima facie case with respect to the above noted limitation. It is further respectfully submitted that Tsinker does not disclose a phase error detecting unit being reset such that the length of the phase error signal has a substantial linear relationship with the phase error of the first input signal and the second input signal. By carefully inspecting Fig.10 of Tsinker, one of ordinary skill in the art would agree that under the situation when the phase difference between the filter clock and the reference clock is less than the delay provided by D1 or D2, the DFFs 206 and 208 will not be involved in the operation of resetting the DFFs 202 and 204. As a result, said linear relationship limitation is not met under such situation. In other words, the phase

comparator 28 taught in Tsinker, unlike the phase frequency detector of the present invention, cannot avoid the so-called dead zone phenomenon.

With regard to Lee, it is noted that Lee fails to teach or suggest a phase frequency detector as set forth in independent claim 1 of the present application, "wherein the phase error detecting unit is reset by the reset signal responsive to an edge of the first input signal, and remains reset for a significant period of time despite of the level of the first input signal after said edge."

By inspecting FIG. 4 of Lee, one of ordinary skill in the art can readily see that the reset status of the DFFs 41 and 42, or the period of time the DFFs maintained reset, is responsive to a logic level (either high or low) of the clock signal REF_CK or CK[7]. In other words, the phase detector shown in FIG. 4 is reset "level-sensitively" in response to the clock signals. However, in the detector disclosed in Figs. 5 or 7 of the present invention the DFFs 401 and 402 are reset and maintain the status of reset upon a rising edge of the input signals Fi and Fr, respectively. In other words, the detector disclosed in the present invention is reset "edge-sensitively" in response to the clock signals.

It is therefore respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the phase frequency detector and phase locked loop of independent claims 1 and 10, as well as their dependent claims. Reconsideration and withdrawal of the 35 USC 102(b) rejections are respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By _____

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